Claims

1. A time-shifted video method comprising

in a real-time mode, delivering real-time video frames for display,

in a time-shifted mode, delivering time-shifted video frames for display, the time-shifted video frames being delayed relative to the real-time video frames, and

pausing a real-time frame in a transition from the real-time mode to the time-shifted mode.

2. The method of claim 1 in which the transition is between the paused real-time frame and a time-shifted version of the paused real-time frame.

3. The method of claim 1 further comprising providing trick functions during the time-shifted mode.

4. The method of claim 1 in which the transition mode is triggered by a command of a viewer or an event generated by software.

5. The method of claim 1 in which the real-time video frames are derived from input uncompressed video.

6. The method of claim 5 in which the real-time video frames are provided from an input frame buffer.

7. The method of claim 1 in which the real-time video frames are derived from input compressed video.

8. The method of claim 7 in which the real-time frames are provided from a decoder that decompresses the input compressed video.

9. The method of claim 1 in which the real-time mode, the time-shifted mode, and the transition are provided by a single codec chip.

10. The method of claim 8 in which the compressed video comprises MPEG video.

11. The method of claim 1 in which information is stored identifying the paused frame, and before the time-shifted mode occurs, the predetermined frame or the next frame after the predetermined frame is queued up.

12. Video apparatus comprising

a port to receive an input video signal,

a time-shifted processing path that stores compressed video frames based on the input video signal and delivers time-shifted stored video frames to an output,

a real-time processing path that delivers real-time video to the output based on the input video signal, and

control circuitry that controls transitions between the real-time video frames and the time-shifted video frames at the output.

13. The apparatus of claim 12 in which the processing paths include two decoders.

14. The two decoders are provided in a single codec.

15. The apparatus of claim 12 in which the processing paths include an encoder and a decoder.

16. The apparatus of claim 12 in which the encoder and decoder or decoders are provided in a single codec.

17. The apparatus of claim 12 in which the processing paths include buffers and the buffers are provided by a common memory.

18. The apparatus of claim 12 in which the video apparatus comprises a set-top box.

19. The apparatus of claim 12 in which the video apparatus comprises an analog television receiver.

20. A set-top box comprising

a compressed digital video input,

a display video output,

a real-time decoder coupled to the input and the output,

a frame storage system coupled to the input,a time-shifted decoder coupled to the frame storage system and the output, and

a controller coupled to the time-shifted decoder, the storage system, and the output.

21. An analog television receiver comprising

an uncompressed video input,

a display video output,

a frame buffer coupled to the input and the output,

a frame storage system coupled to the input,

a time-shifted decoder coupled to the output, and

a controller coupled to the time-shifted decoder, the storage system, and the output.

22. A set-top box comprising

a compressed digital video input,

an uncompressed video input,

a display video output,

a real-time decoder coupled to the input and the output,

a frame storage system coupled to the input,

a time-shifted decoder coupled to the frame storage system and the output, and

a controller coupled to the time-shifted decoder, the storage system, and the output.

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